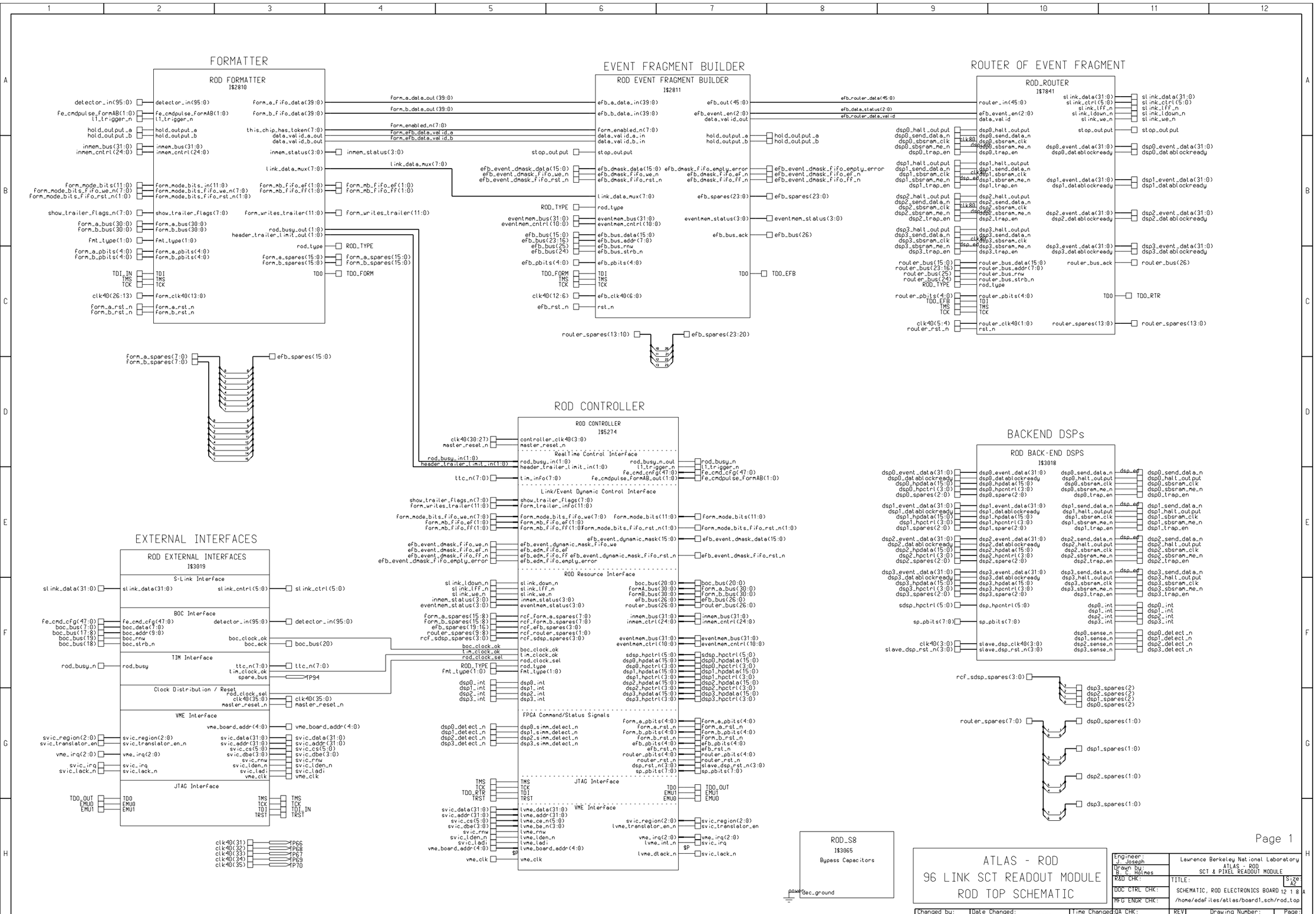
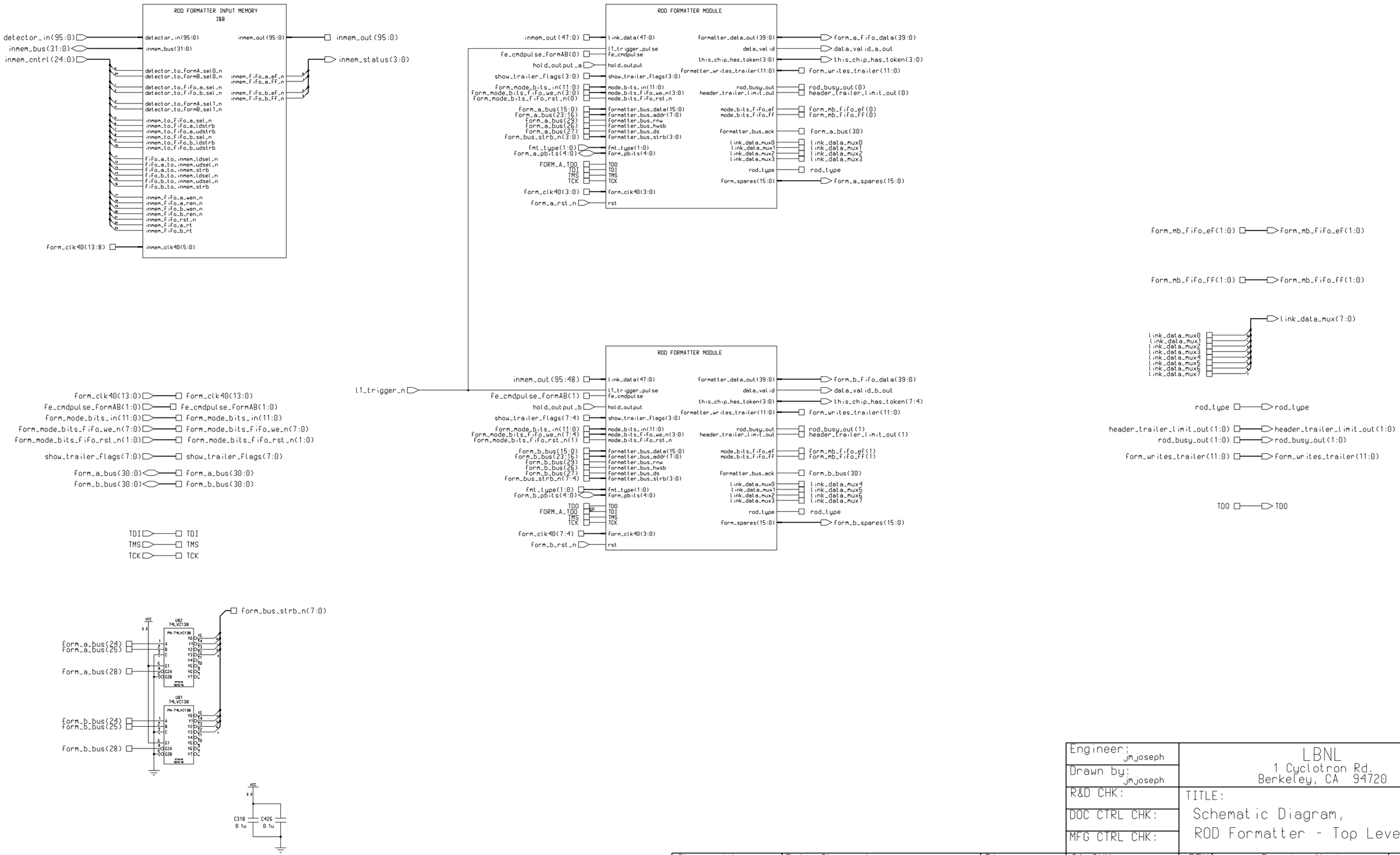
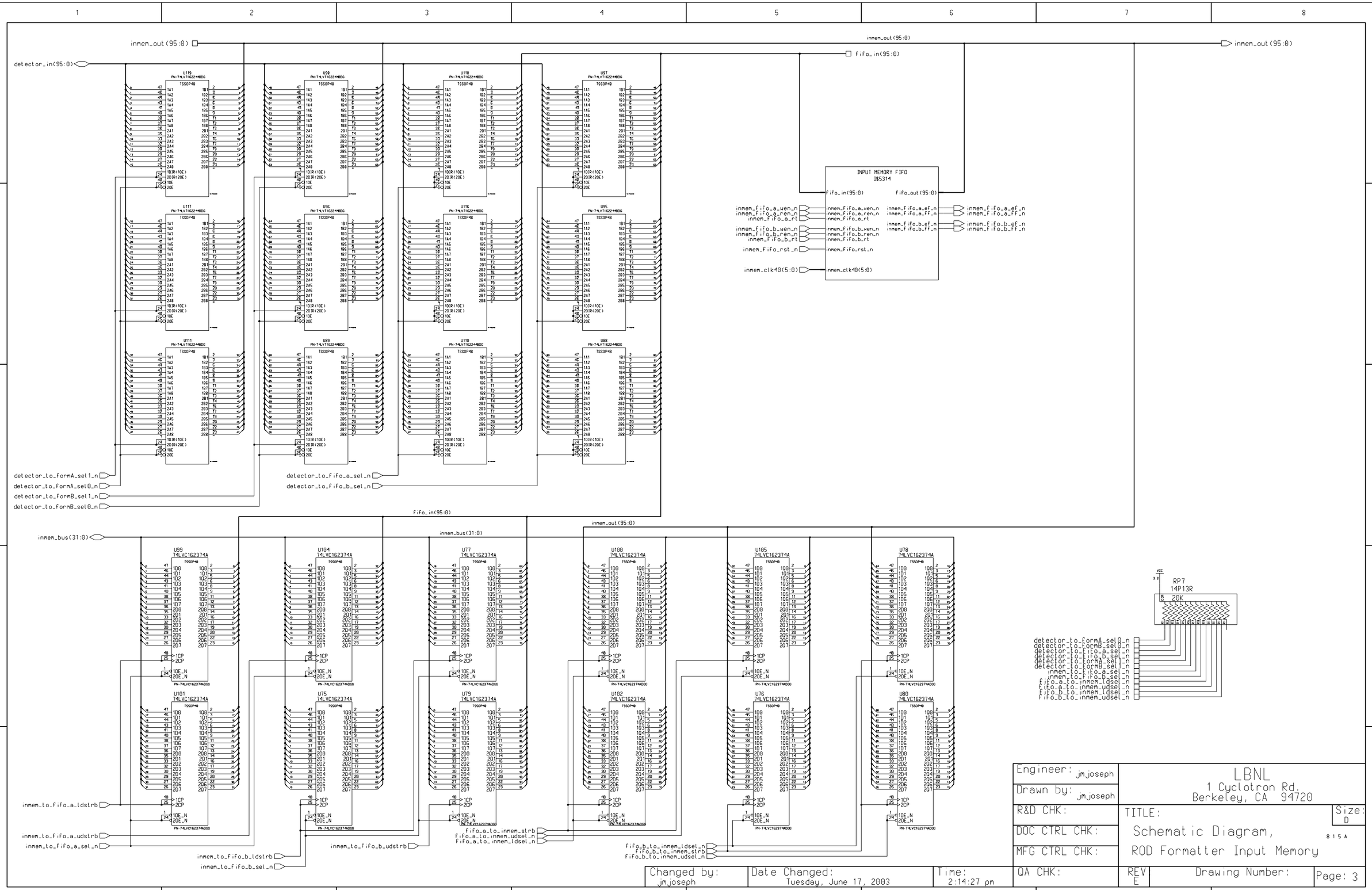
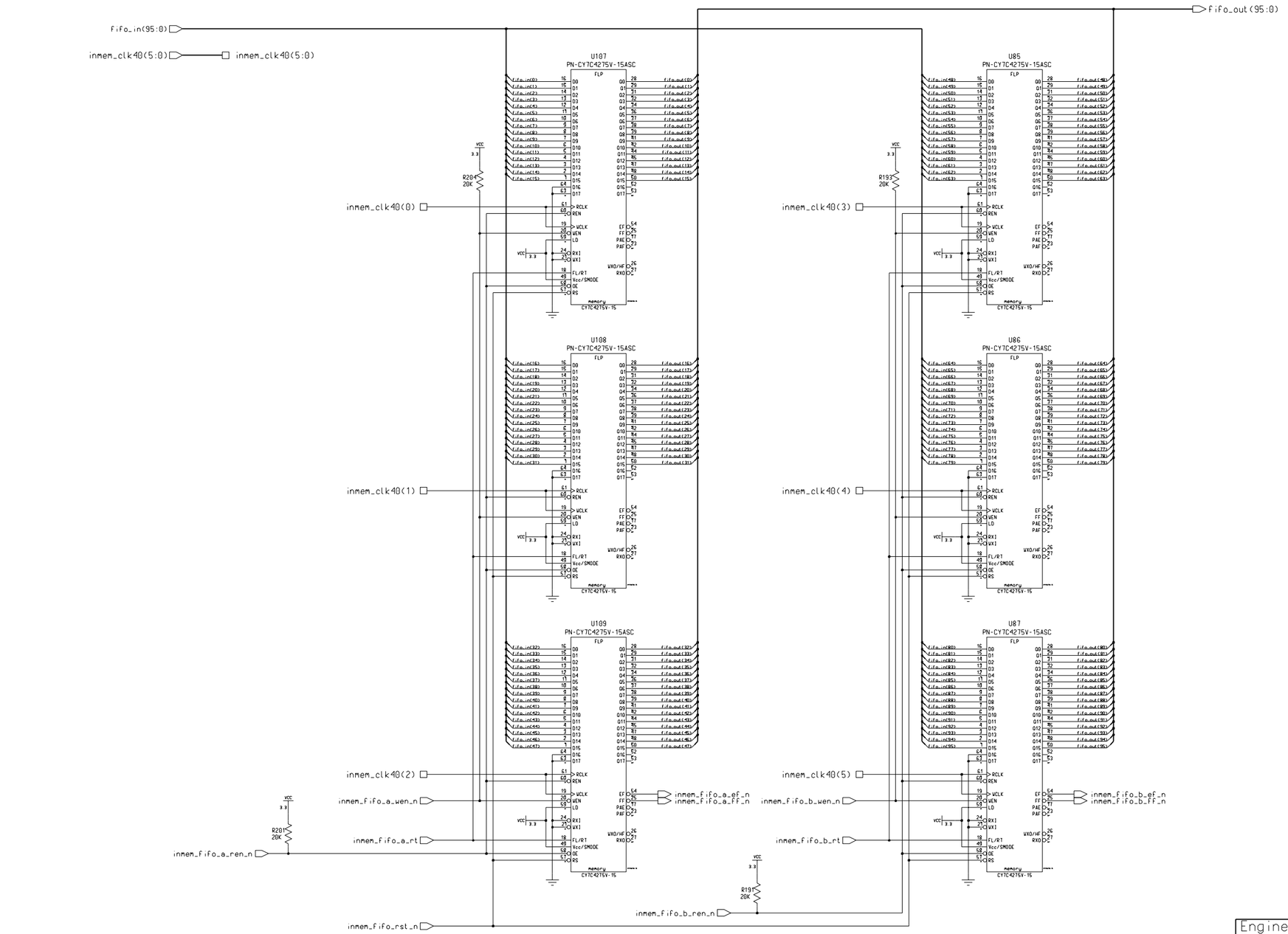

FORMATTER
ROD FORMATTER
I$2810
EVENT FRAGMENT BUILDER
ROD EVENT FRAGMENT BUILDER
I$2811
ROUTER OF EVENT FRAGMENT
ROD_ROUTER
I$7841
ROD CONTROLLER
ROD CONTROLLER
I$5274
Realtime Control Interface
Link/Event Dynamic Control Interface
ROD Resource Interface
FPGA Command/Status Signals
JTAG Interface
VME Interface
BACKEND DSPs
ROD BACK-END DSPS
I$3018
EXTERNAL INTERFACES
ROD EXTERNAL INTERFACES
I$3019
S-Link Interface
BOC Interface
TIM Interface
Clock Distribution / Reset
VME Interface
JTAG Interface
ROD_S8
I$3065
Bypass Capacitors
Page 1
ATLAS - ROD
96 LINK SCT READOUT MODULE
ROD TOP SCHEMATIC
Engineer: J. Joseph
Drawn by: B. C. Holmes
Lawrence Berkeley National Laboratory
ATLAS - ROD
SCT & PIXEL READOUT MODULE
TITLE:
SCHEMATIC, ROD ELECTRONICS BOARD
/home/edafiles/atlas/board1_sch/rod_top
Size: A2
Changed by: jmjoseph
Date Changed: Tuesday, June 17, 2003
Time Changed: 2:16:20 pm
Drawing Number:
Page: 1

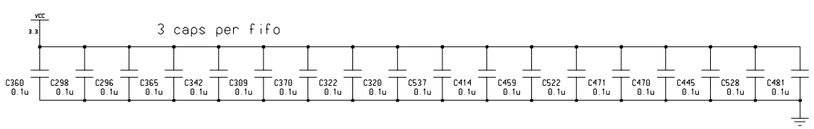


Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Formatter - Top Level	Size: D 815A	
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV E	Drawing Number:	Page: 2

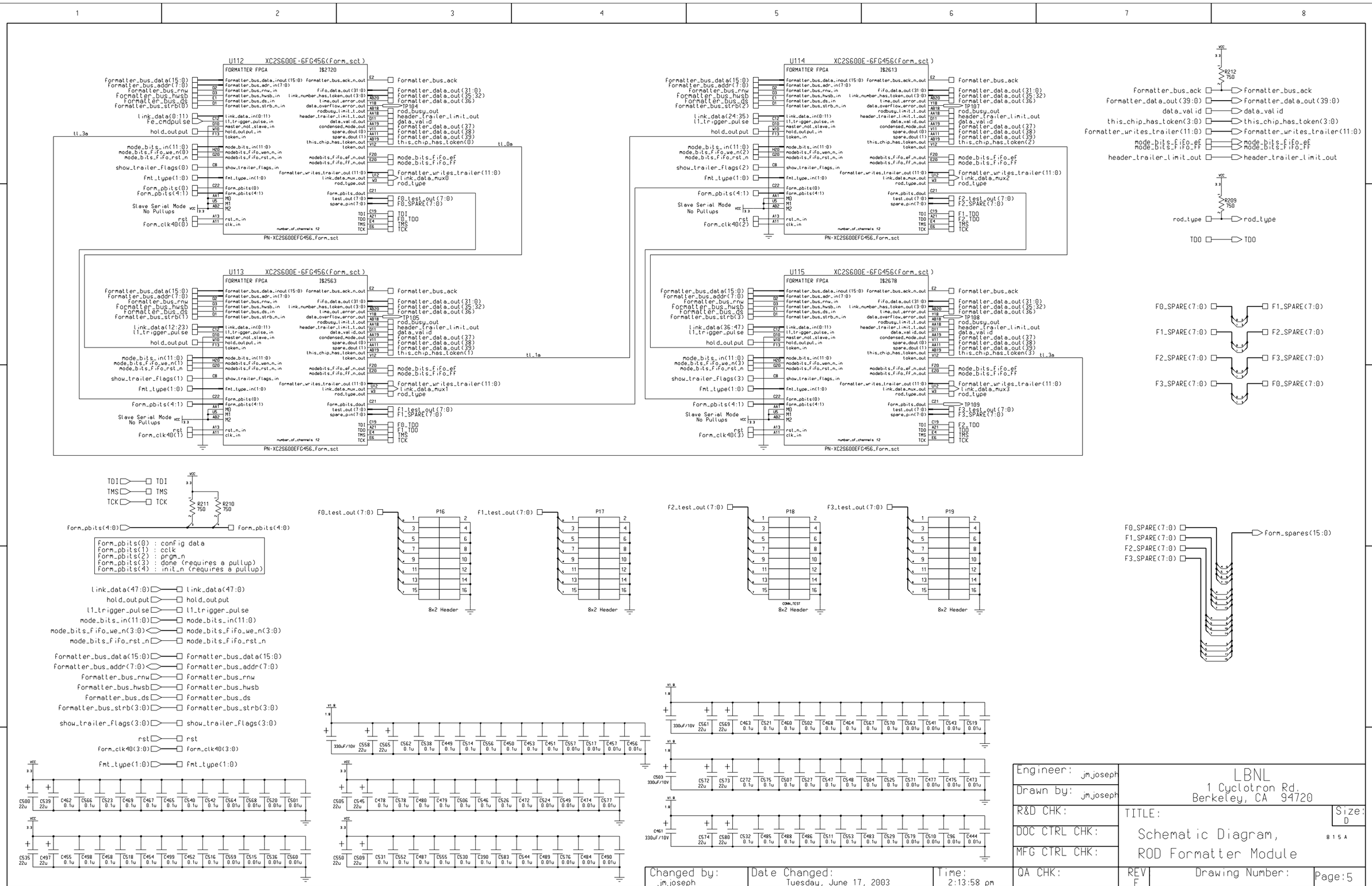
Changed by:	Date Changed:	Time:
jmjoseph	Tuesday, June 17, 2003	2:14:40 pm


inmem_out(95:0)
detector_in(95:0)
Fifo_in(95:0)
INPUT MEMORY FIFO
IS5314
fifo_in(95:0)
fifo_out(95:0)
inmem_fifo_a_wen_n
inmem_fifo_a_ren_n
inmem_fifo_a_rt
inmem_fifo_b_wen_n
inmem_fifo_b_ren_n
inmem_fifo_b_rt
inmem_fifo_rst_n
inmem_clk40(5:0)
inmem_fifo_a_ef_n
inmem_fifo_a_ff_n
inmem_fifo_b_ef_n
inmem_fifo_b_ff_n
detector_to_formA_sel1_n
detector_to_formA_sel0_n
detector_to_formB_sel1_n
detector_to_formB_sel0_n
detector_to_fifo_a_sel_n
detector_to_fifo_b_sel_n
inmem_bus(31:0)
RP7
14P13R
20K
inmem_to_fifo_a_ldstrb
inmem_to_fifo_a_udstrb
inmem_to_fifo_a_sel_n
inmem_to_fifo_b_ldstrb
inmem_to_fifo_b_sel_n
inmem_to_fifo_b_udstrb
fifo_a_to_inmem_strb
fifo_a_to_inmem_udsel_n
fifo_a_to_inmem_ldsel_n
fifo_b_to_inmem_ldsel_n
fifo_b_to_inmem_strb
fifo_b_to_inmem_udsel_n
Engineer: jmjoseph
Drawn by: jmjoseph
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
LBNL
1 Cyclotron Rd.
Berkeley, CA 94720
TITLE:
Schematic Diagram,
ROD Formatter Input Memory
Size: D
815A
Changed by: jmjoseph
Date Changed: Tuesday, June 17, 2003
Time: 2:14:27 pm
QA CHK:
REV E
Drawing Number:
Page: 3



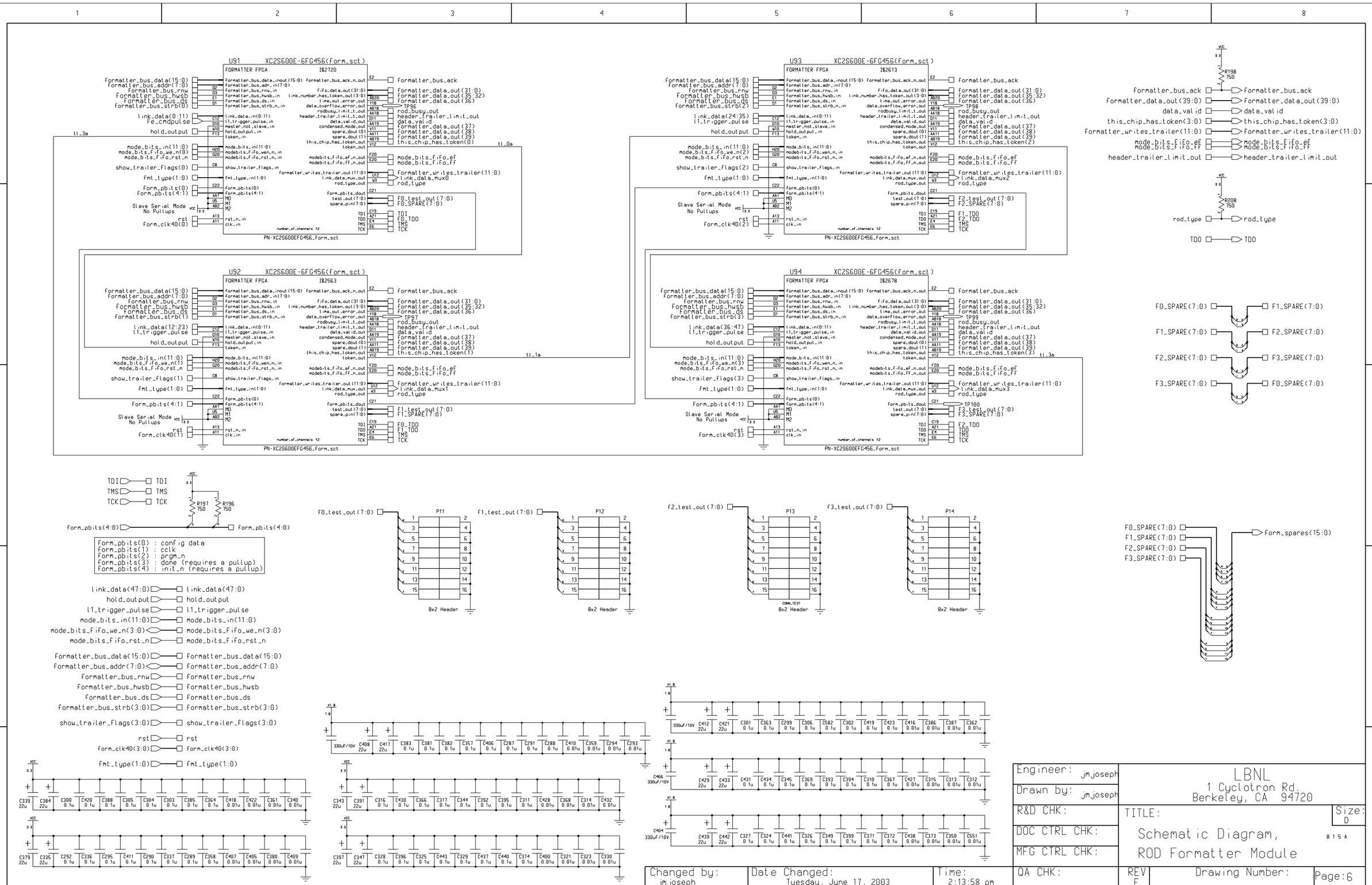


Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE:	Size: D	
DOC CTRL CHK:	Schematic Diagram,	815A	
MFG CTRL CHK:	ROD Formatter Input Memory FIFO		
Changed by: jmjoseph	Date Changed: Tuesday, June 17, 2003	Time: 2:14:21 pm	QA CHK:
REV E	Drawing Number:	Page: 4	



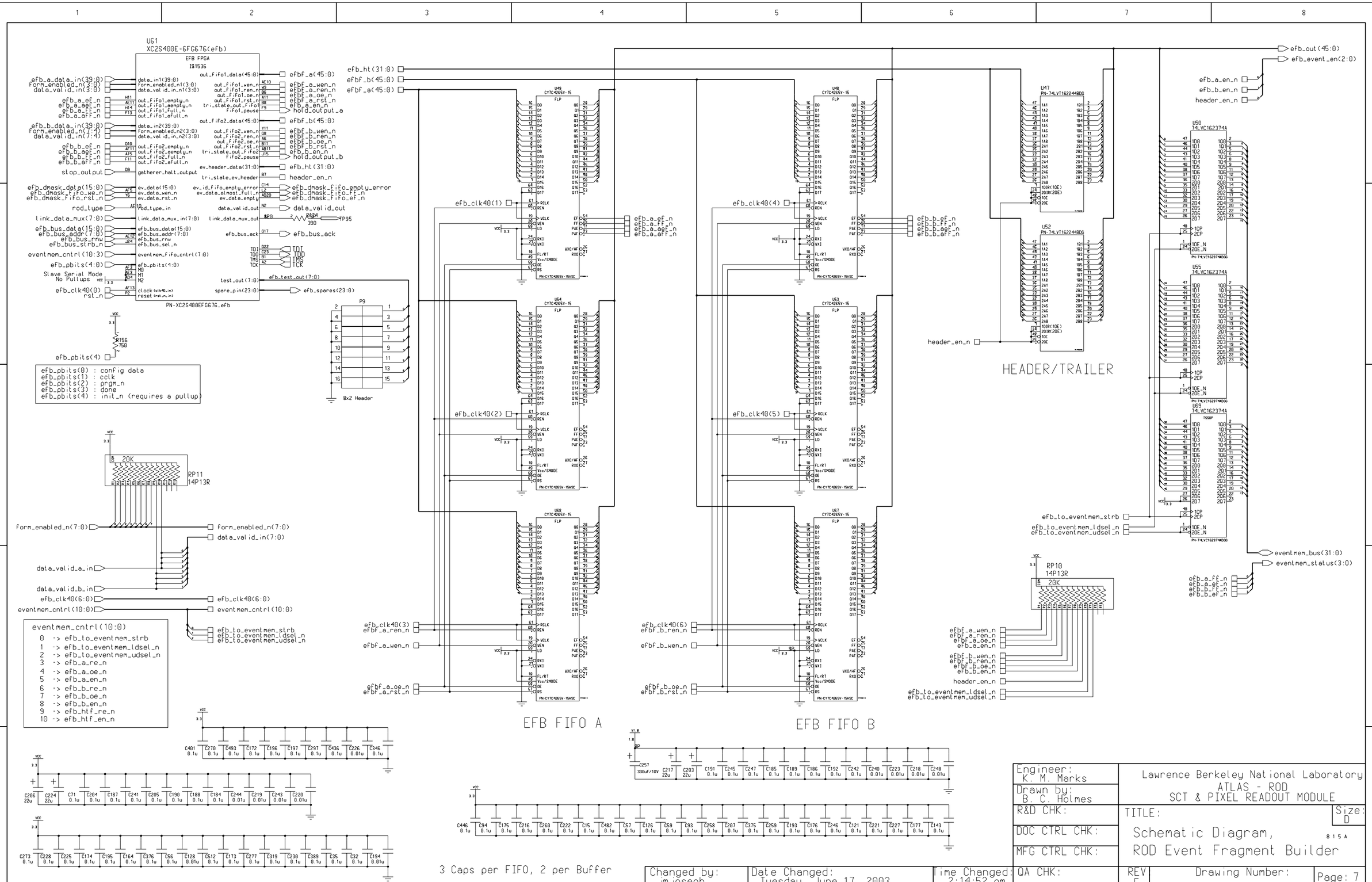
Changed by: jmjoseph	Date Changed: Tuesday, June 17, 2003	Time: 2:13:58 pm	QA CHK:

Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720	
Drawn by: jmjoseph		
R&D CHK:	TITLE:	Size: D
DOC CTRL CHK:	Schematic Diagram,	8 1 5 A
MFG CTRL CHK:	ROD Formatter Module	
REV E	Drawing Number:	Page:5



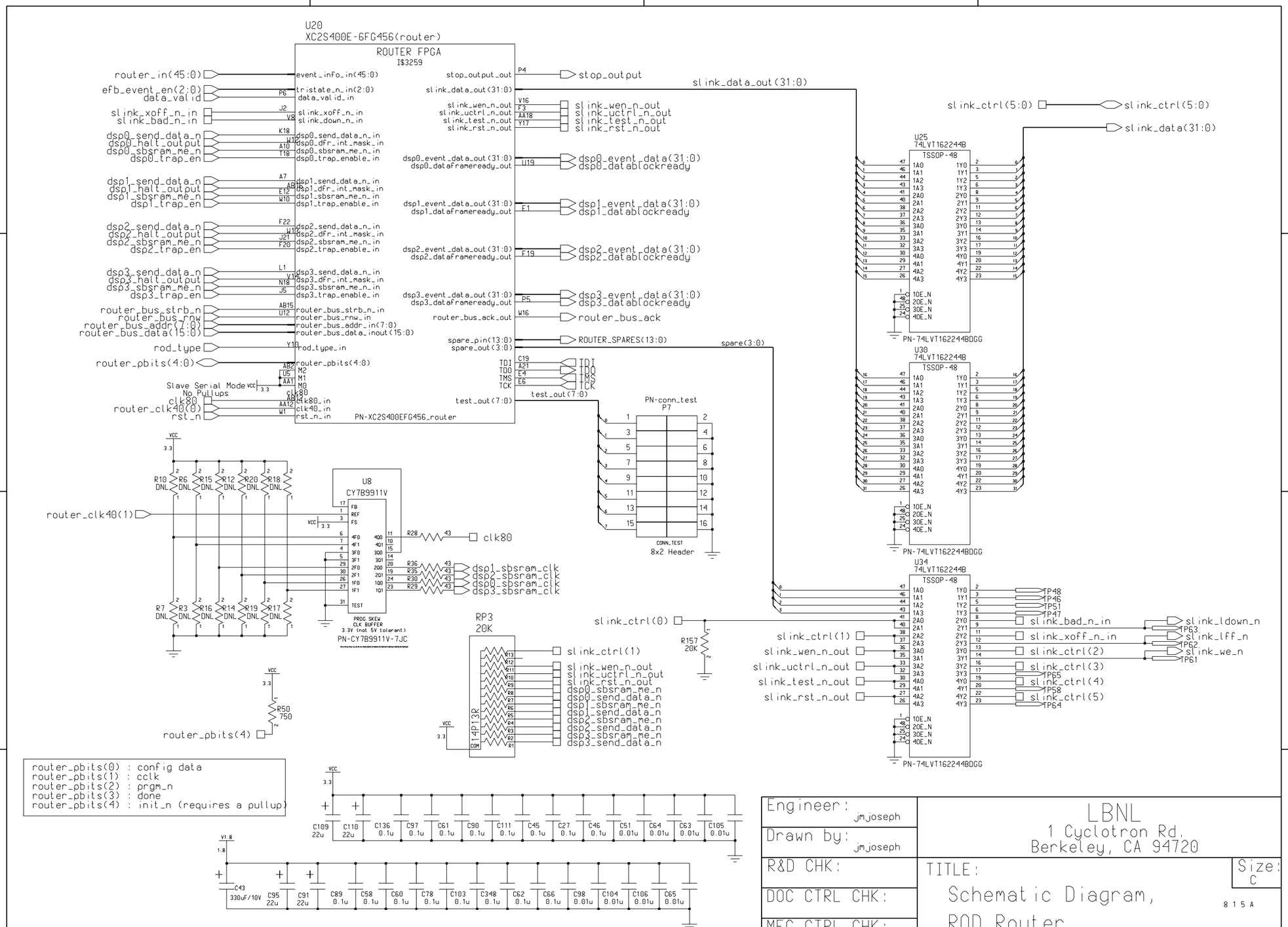
Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE:	Size: D	
DOC CTRL CHK:	Schematic Diagram,	8 1 5 A	
MFG CTRL CHK:	ROD Formatter Module		
QA CHK:	REV E	Drawing Number:	Page:6

Changed by:	Date Changed:	Time:
jmjoseph	Tuesday, June 17, 2003	2:13:58 pm



Engineer: K. M. Marks	Lawrence Berkeley National Laboratory ATLAS - ROD SCT & PIXEL READOUT MODULE		
Drawn by: B. C. Holmes			
R&D CHK:	TITLE:		Size: D
DOC CTRL CHK:	Schematic Diagram,		815A
MFG CTRL CHK:	ROD Event Fragment Builder		
QA CHK:	REV E	Drawing Number:	Page: 7

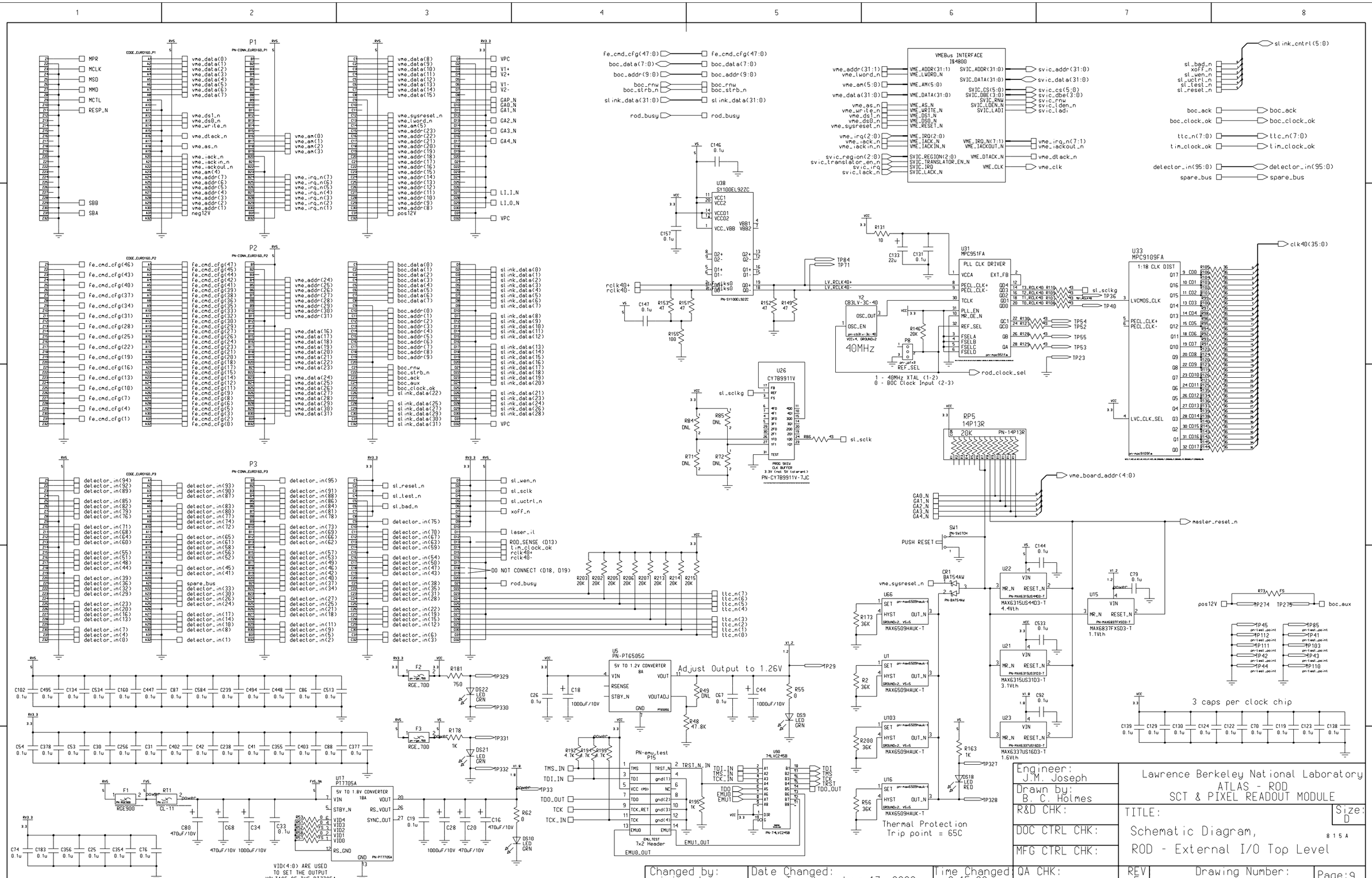
Changed by:	Date Changed:	Time Changed:
jmjoseph	Tuesday, June 17, 2003	2:14:52 pm



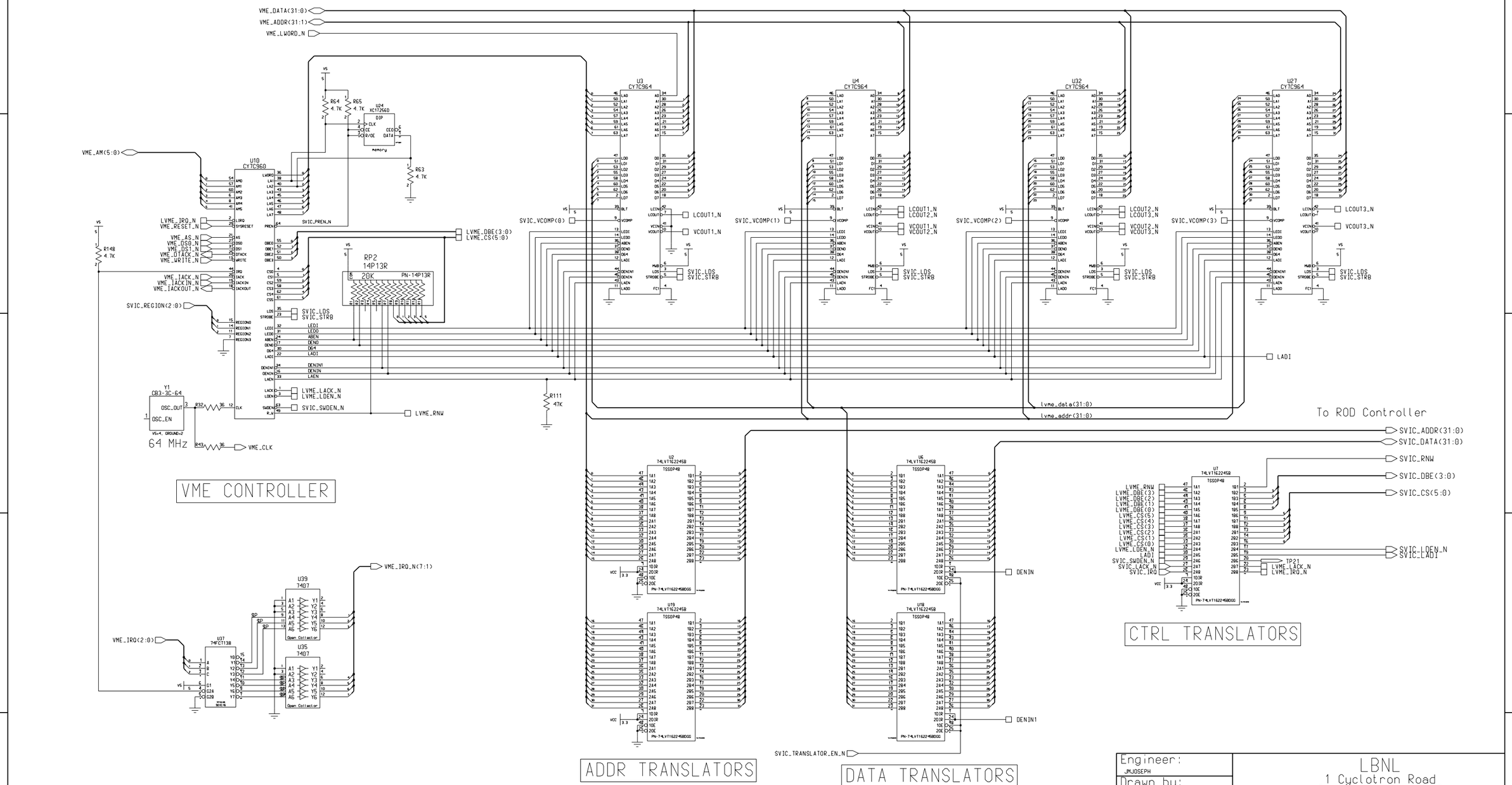
router_pbits(0) : config data
router_pbits(1) : cclk
router_pbits(2) : prgm_n
router_pbits(3) : done
router_pbits(4) : init_n (requires a pullup)

Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720	
Drawn by: jmjoseph		
R&D CHK:	TITLE: Schematic Diagram, ROD Router	Size: C 815A
DOC CTRL CHK:		
MFG CTRL CHK:		
QA CHK:	REV: E Drawing Number:	Page: 8

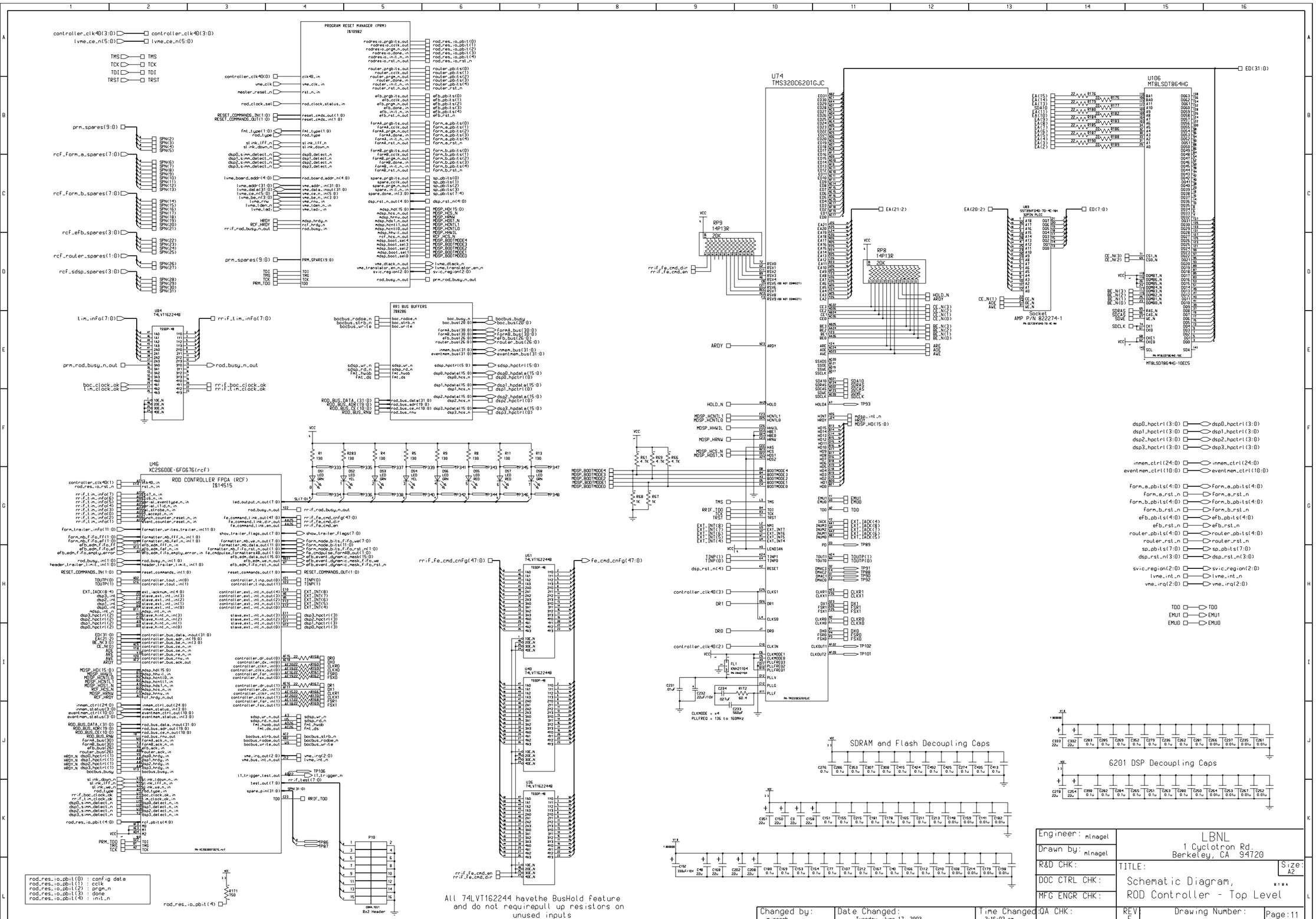
Changed by:	Date Changed:	Time:
jmjoseph	Tuesday, June 17, 2003	2:15:06 pm

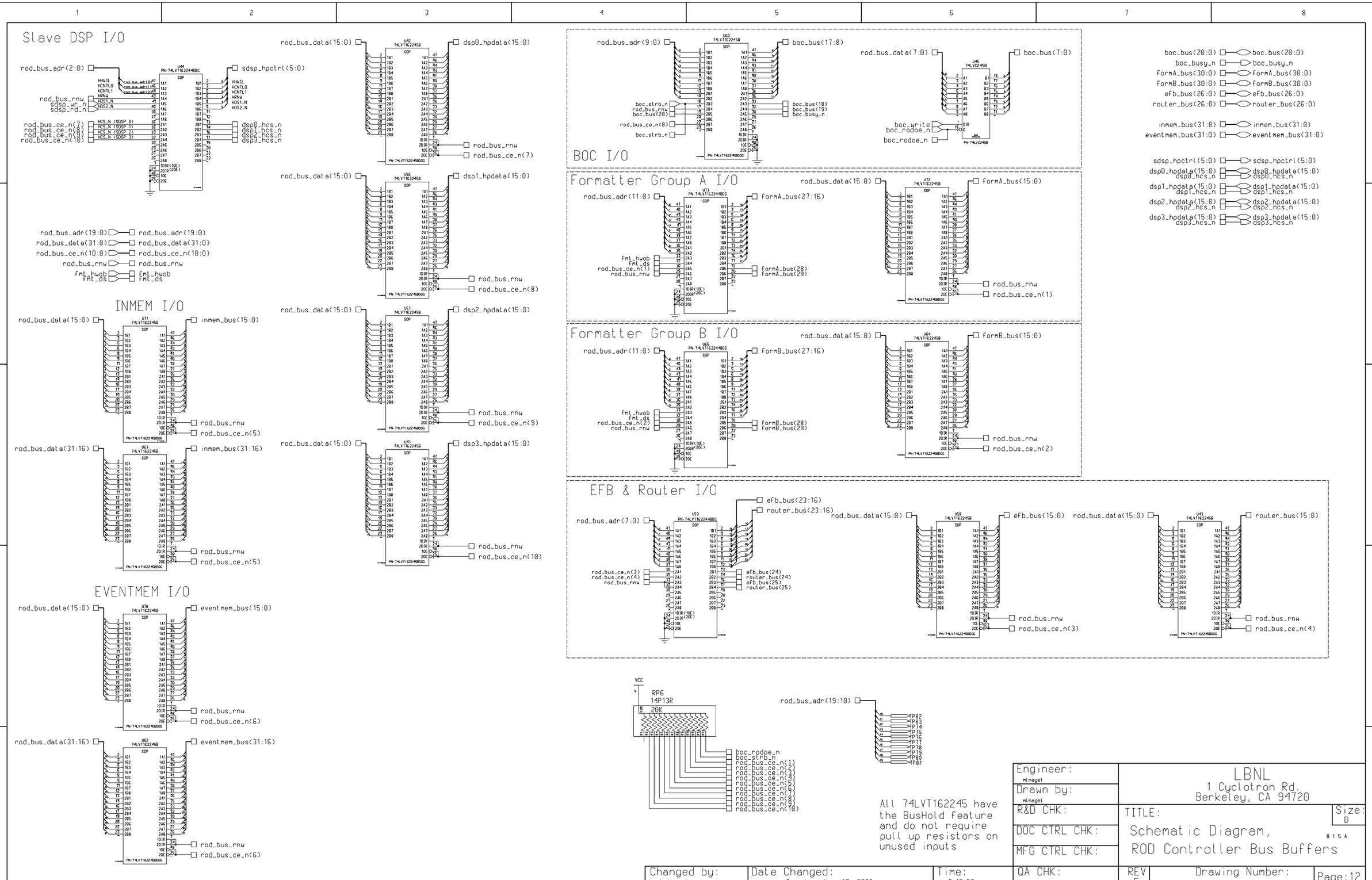

P1
P2
P3
VMEBus INTERFACE
IS4800
U38
SY100EL92ZC
U31
MPC951FA
PLL CLK DRIVER
U33
MPC9109FA
1:18 CLK DIST
U26
CY7B9911V
U17
PT7705A
5V TO 1.8V CONVERTER
U5
PT6505G
5V TO 1.2V CONVERTER
Adjust Output to 1.26V
U99
74LVC245B
RP5
14P13R
U22
U21
U23
U15
U66
U1
U103
U16
MAX6509HAUK-T
MAX6315US44D3-T
4.4Vth
MAX6315US31D3-T
3.1Vth
MAX6337US16D3-T
1.6Vth
MAX6837FXSD3-T
1.1Vth
Thermal Protection
Trip point = 65C
3 caps per clock chip
VID(4:0) ARE USED
TO SET THE OUTPUT
VOLTAGE OF THE PT7705A
Engineer:
J.M. Joseph
Drawn by:
B. C. Holmes
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
Lawrence Berkeley National Laboratory
ATLAS - ROD
SCT & PIXEL READOUT MODULE
TITLE:
Schematic Diagram,
ROD - External I/O Top Level
Size:
D
Changed by:
jmjoseph
Date Changed:
Tuesday, June 17, 2003
Time Changed:
2:15:28 pm
QA CHK:
REV
E
Drawing Number:
Page:9

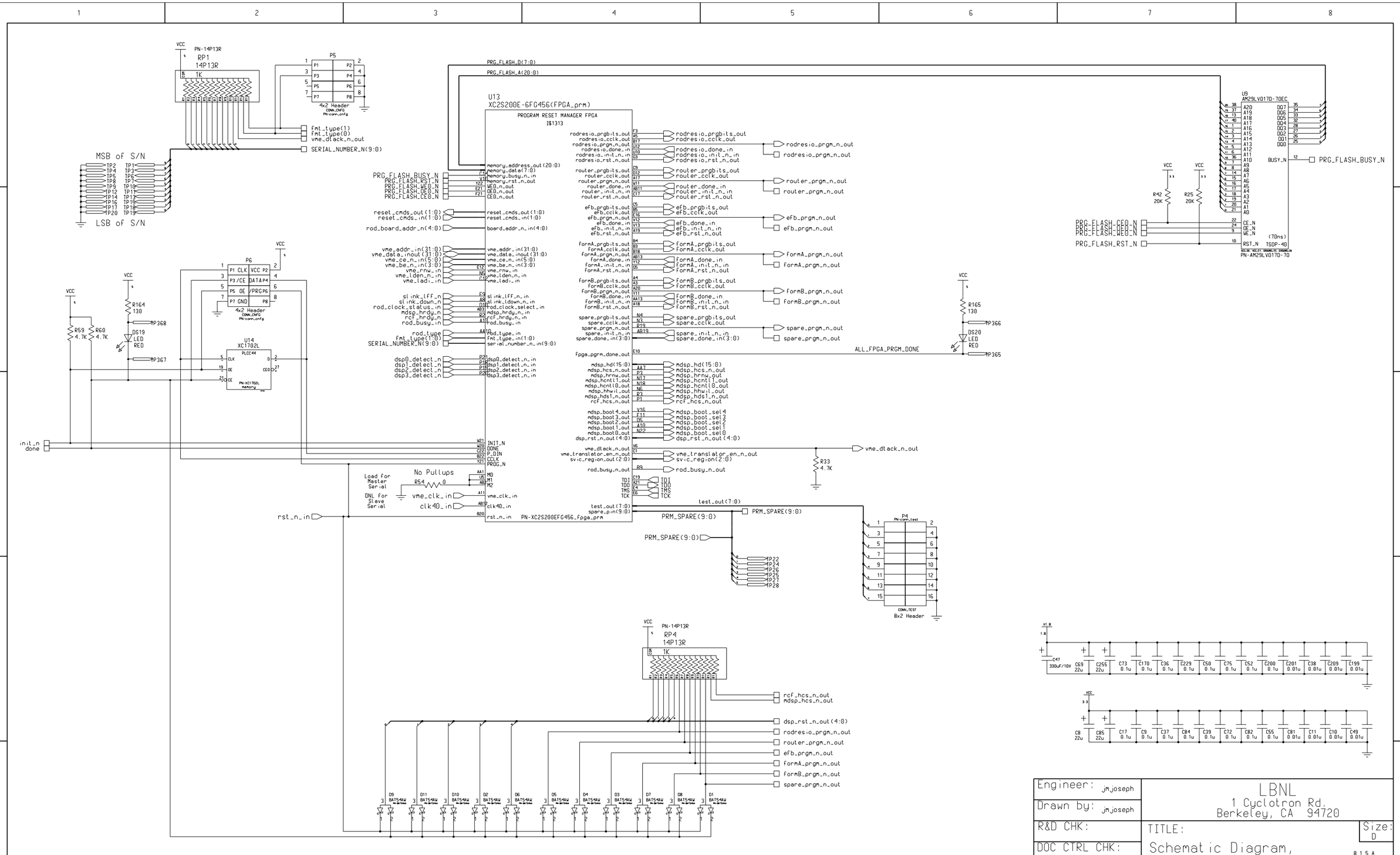
VME TRANSCEIVERS



Engineer: JMJOSEPH	LBNL 1 Cyclotron Road Berkeley, CA 94720		
Drawn by: JMJOSEPH			
R&D CHK:	TITLE: Schematic Diagram, ROD VME Interface	Size: D	414A
DOC CTRL CHK:			
MFG ENGR CHK:			
Changed by: jmjoseph	Date Changed: Tuesday, June 17, 2003	Time Changed: 2:15:22 pm	QA CHK:
REV E	Drawing Number:	Page:10	

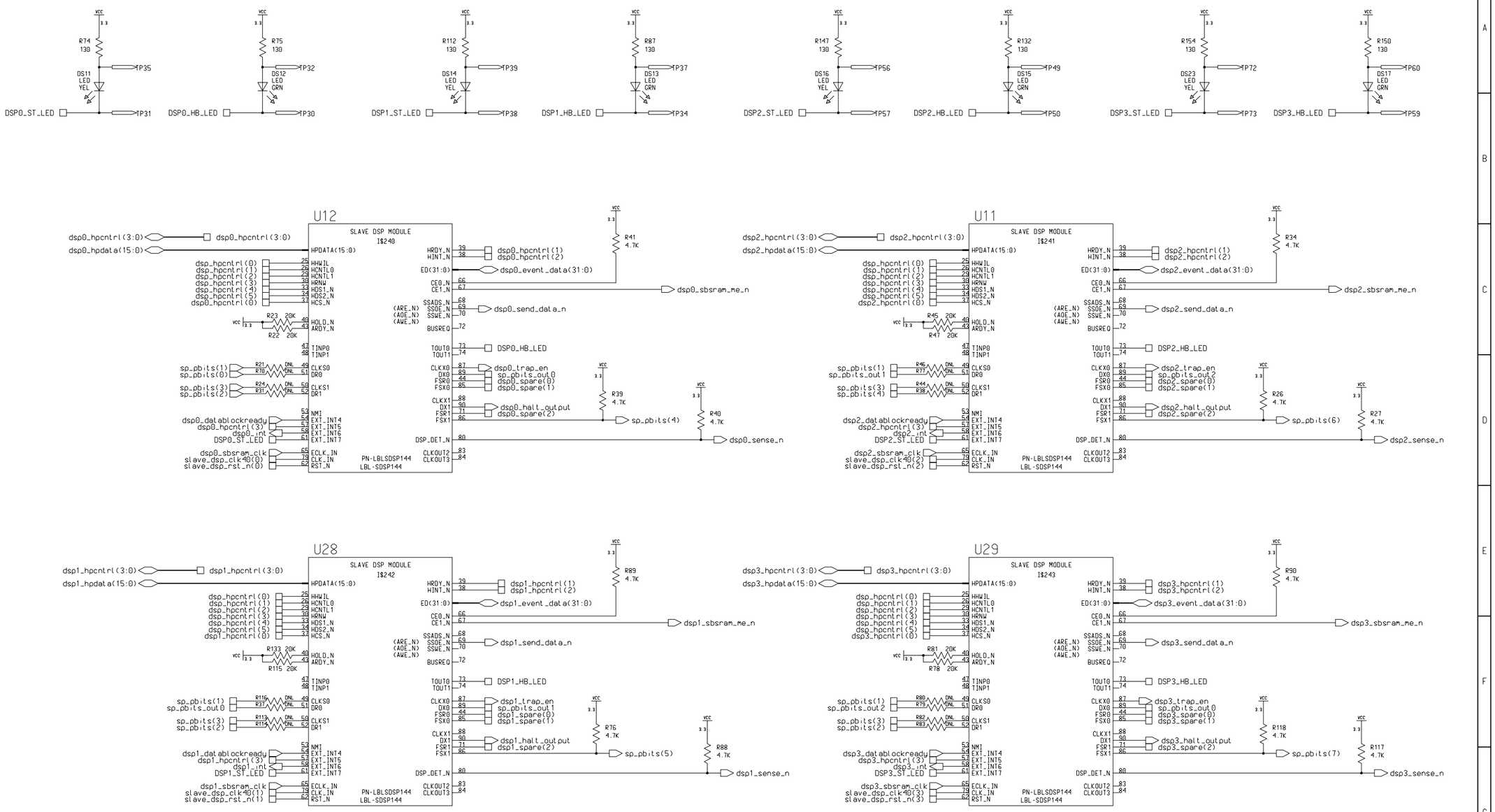

PROGRAM RESET MANAGER (PRM)
IS10982
ROD CONTROLLER FPGA (RCF)
IS14515
U74
TMS320C6201GJC
U106
MT8LSDT864HG
MT8LSDT864HG-10EC5
U84
74LVT162244B
R91 BUS BUFFERS
IS8286
U46
XC2S600E-6FG676(rcf)
U51
74LVT162244B
U40
74LVT162244B
U36
74LVT162244B
RP9
14P13R
20K
RP8
14P13R
20K
U93
SST39VF040-70-4C-NH
32PIN PLCC
Socket
AMP P/N 822274-1
PM-SST39VF040-70-4C-NH
PM-MT8LSDT864HG-10EC5
PM-TMS320C6201GJC
PM-XC2S600E-6FG676(rcf)
PM-MT8LSDT864HG-100EC5
P10
8x2 Header
SDRAM and Flash Decoupling Caps
6201 DSP Decoupling Caps
controller_clk40(3:0)
lvme_ce_n(5:0)
TMS
TCK
TDI
TRST
prm_spares(9:0)
rcf_form_a_spares(7:0)
rcf_form_b_spares(7:0)
rcf_efb_spares(3:0)
rcf_router_spares(1:0)
rcf_sdsp_spares(3:0)
lim_info(7:0)
rrif_lim_info(7:0)
prm_rod_busy_n_out
rod_busy_n_out
boc_clock_ok
lim_clock_ok
rrif_boc_clock_ok
rrif_lim_clock_ok
rod_res_io_pbit(0) : config data
rod_res_io_pbit(1) : cclk
rod_res_io_pbit(2) : prgm_n
rod_res_io_pbit(3) : done
rod_res_io_pbit(4) : init_n
All 74LVT162244 havethe BusHold feature
and do not requirepull up resistors on
unused inputs
Engineer: mlnagel
Drawn by: mlnagel
R&D CHK:
DOC CTRL CHK:
MFG ENGR CHK:
LBNL
1 Cyclotron Rd.
Berkeley, CA 94720
TITLE:
Schematic Diagram,
ROD Controller - Top Level
Size: A2
QA CHK:
REV -E
Drawing Number:
Page:11
Changed by: jm_joseph
Date Changed: Tuesday, June 17, 2003
Time Changed: 2:16:02 pm


Slave DSP I/O
INMEM I/O
EVENTMEM I/O
BOC I/O
Formatter Group A I/O
Formatter Group B I/O
EFB & Router I/O
RP6
14P13R
20K
VCC
All 74LVT162245 have the BusHold feature and do not require pull up resistors on unused inputs
Engineer: mlnagel
Drawn by: mlnagel
R&D CHK:
DOC CTRL CHK:
MFG CTRL CHK:
QA CHK:
LBNL
1 Cyclotron Rd.
Berkeley, CA 94720
TITLE:
Schematic Diagram,
ROD Controller Bus Buffers
Size: D
815A
REV E
Drawing Number:
Page:12
Changed by: jmjoseph
Date Changed: Tuesday, June 17, 2003
Time: 2:15:53 pm



Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720
Drawn by: jmjoseph	
R&D CHK:	TITLE: Schematic Diagram, ROD Program and Reset Manager
DOC CTRL CHK:	Size: D
MFG CTRL CHK:	815A
QA CHK:	REV E — Drawing Number: — Page:13

Changed by:	Date Changed:	Time:
jmjoseph	Tuesday, June 17, 2003	2:15:44 pm



dsp0_spare(2:0) — dsp0_spare(2:0)
dsp1_spare(2:0) — dsp1_spare(2:0)
dsp2_spare(2:0) — dsp2_spare(2:0)
dsp3_spare(2:0) — dsp3_spare(2:0)
slave_dsp_clk40(3:0) — slave_dsp_clk40(3:0)
slave_dsp_rst_n(3:0) — slave_dsp_rst_n(3:0)
dsp_hpcntrl(5:0) — dsp_hpcntrl(5:0)

sp_pbits(0) : config data
sp_pbits(1) : cclk
sp_pbits(2) : prgm_n
sp_pbits(3) : init_n (requires a pullup)
sp_pbits(4:7) : done

Engineer: jmjoseph	LBNL 1 Cyclotron Rd. Berkeley, CA 94720		
Drawn by: jmjoseph			
R&D CHK:	TITLE: Schematic Diagram, ROD Slave DSP Top	Size: A2	
DOC CTRL CHK:			
MFG CTRL CHK:			
QA CHK:	REV: E	Drawing Number:	Page:14

Changed by: jmjoseph | Date Changed: Tuesday, June 17, 2003 | Time: 2:16:12 pm